1. A process for forming copper metal interconnects and copper-filled vias in a dielectric layer on an integrated circuit structure wherein the impurity level of the copper-filled metal lines and copper-filled vias is lowered, the process comprising:

a) depositing a layer of copper metal in trenches and via openings previously formed in one or more dielectric layers;

b) then annealing the deposited copper layer;

c) then optionally removing a thin portion of the top surface of the deposited copper layer;

d) then repeating at least the deposit step and the step of annealing the deposited layer of copper one or more additional times; and

e) then planarizing the annealed structure.

2. The process of claim 1 including the further step of annealing the planarized structure.

3. The process of claim 2 wherein said copper layer is annealed at a temperature within a range of from about 150°C to about 400°C.

4. The process of claim 3 wherein said copper layer is annealed in a furnace for a period of from about 0.5 minutes to about 30 minutes.

5. The process of clam 3 wherein said copper layer is annealed using rapid thermal annealing.

6. A process for forming copper metal interconnects and copper-filled vias in a dielectric layer on an integrated circuit structure wherein the impurity level of the copper-filled metal lines and copper-filled vias is lowered, the process comprising:

a) depositing a layer of copper metal in trenches and via openings previously formed in one or more dielectric layers;

b) then annealing the deposited copper layer;

c) then removing a thin portion of the surface of said deposited copper layer;

d) then repeating the depositing step, the annealing step, and the removing step one additional time; and

e) then planarizing the annealed structure;

whereby the average grain size of the copper is increased, the resistivity is reduced, and stresses are more homogeneously distributed in the copper.

7. The process of claim 6 including the further step of annealing the planarized structure.

8. The process of claim 7 wherein said copper layer is annealed at a temperature within a range of from about 150°C to about 400°C.

9. The process of claim 8 wherein said copper layer is annealed in a furnace for a period of from about 0.5 minutes to about 30 minutes.

10. The process of clam 8 wherein said copper layer is annealed using rapid thermal annealing.

11. A process for forming copper metal interconnects and copper-filled vias in a dielectric layer on an integrated circuit structure wherein the impurity level of the copper-filled metal lines and copper-filled vias is lowered, the process comprising:

a) depositing a layer of copper metal in trenches and via openings previously formed in one or more dielectric layers;

b) then annealing the deposited copper layer;

c) then, removing a thin portion of copper from the surface of said deposited copper layer;

d) then repeating steps a, b, and c one or more additional times to complete the filling of the trenches and vias with copper; and

e) then planarizing the structure.

12. The process of claim 11 including the further step of annealing the planarized structure.

13. The process of claim 11 including the further steps of:

a) depositing a further layer of copper metal over said filled trenches and via openings previously formed in said one or more dielectric layers; and

b) then annealing said further layer of copper.

14. The process of claim 13 wherein said further layer of copper is annealed at a temperature within a range of from about 150°C to about 400°C.

15. The process of claim 14 wherein said further layer of copper is annealed in a furnace for a period of from about 0.5 minutes to about 5 minutes.

16. The process of clam 14 wherein said further layer of deposited copper is annealed using rapid thermal annealing.